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A REVIEW OF PARAMETRIC OPTIMIZATION FOR CMOS VOLTAGE CIRCUIT

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ABSTRACT:
With the advancement of CMOS technology, the size of the MOSFET device decreases. The study is conducted to summarize the circuit techniques and technologies used in the development of circuits. It also checks the problems solved by the circuits. Enhance circuit coding to automatically generate structure and differential expansion algorithm to efficiently optimize parameters. Enhance the circuit coding method and extend the instruction set on the fly. The circuit designer finds optimum performance through precise calculations and parameterizations, which take time and effort, and the automatic design would help the designer easily find the optimum point. Therefore, automatic design is required for analog integrated circuits. This article introduces the intended CMOS voltage reference circuit and the voltage reference circuit principle. A brief overview of the voltage reference architecture and current reference architecture is described.
Keywords: CMOS, MOSFET, Integrated Circuits, VREF**.**

INTRODUCTION

There are many written provisions for generating a reference voltage. A common approach is to use a bandgap reference that can be implemented in any standard CMOS innovation that abuses spurious vertical BJTs [1, 2]. Other voltage references abuse the limit voltage contrast guidelines, which may be based on the inclusion of some channels [3, 4], differentiation of the level band voltage from different input materials [5] and the working contrast obtained from the characteristic doping at the entrance [6].

These arrangements cannot be upgraded in a standard CMOS innovation because they require additional manufacturing steps. A further type of voltage reference obtained with the standard CMOS innovation depends on the weighted differentiation of the input voltage source between an NMOS transistor and a PMOS [7]. In this article, we look at a voltage reference that can be implemented in any standard CMOS innovation in terms of the voltage contrast of the weighted gate source between two NMOS transistors. Fig. 1 shows a base voltage reference generator using MOS logic.

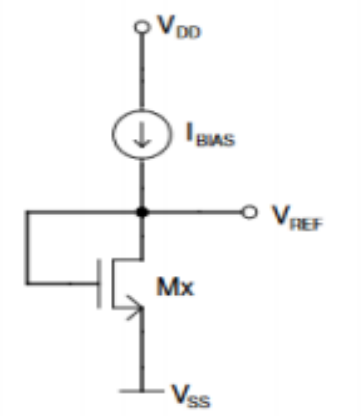

Fig. 1: Voltage Reference Generator

The primary standard for most MOSFET voltage references is to have at least one MOSFET with an existing generator with a single temperature dependence to generate the reference voltage (VREF). The main topology is shown in Fig.1.

This generator discharges the control power. Considering the high linearity of the on-board voltage of a MOSFET (VT) as a component of the maximum temperature (T), the obtained reference voltage largely corresponds to the time of V0, the extrapolation of VT (T) to 0 K (Fig. 2), which essentially determines the basic supply voltage.

Some plans overcome this obstacle by using two NMOS transistors with different limit voltages. However, this component is not available in all manufacturing innovations. Recently, a reference has been proposed for discriminating the limiting voltage in two transistors of similar type and of different size.

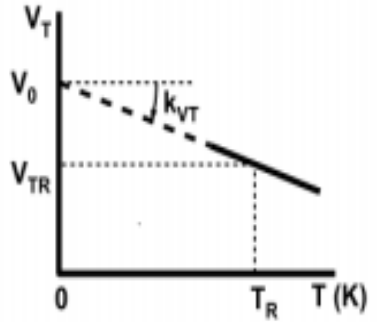

Fig. 2: Temperature Dependence of threshold voltage Vt

The temperature reliability of the VTH reference thusly relies upon the temperature reliance of the biasing current.

LITERATURE REVIEW

Y. Zeng et al. (2017) In a standard 0.18 μm CMOS process, a benchmark was implemented for a voltage below 1V and extremely low power consumption without the use of special resistors and threshold voltage devices. A temperature coefficient (TC) of 37.8 ppm / ° C is obtained in a temperature range from -40 ° C to 60 ° C. The supply voltage is between 1 V and 3 V and the

sensitivity of the line (LS) is 0.02% / V. When V DD is minimum, the measured supply current at ambient temperature is 86 nA and the filter capacitor-less power rejection ratios (PSRR) at 100 Hz and 10 MHz are below -56 dB or -9.5 dB.

Subhash Patel et al. (2016)In this paper proposed an optimizer based on a modified PSO algorithm for the design of automatic circuits. The performance of the modified PSO algorithm is compared with two other evolutionary algorithms, namely the ABC algorithm and the standard PSO algorithm, by designing a two-stage CMOS operational amplifier and a mass control OTA with 130nm technology. The results show the robustness of the proposed algorithm. With the modified PSO algorithm, the mean design error for a two-stage op amp is only 0.054% compared to 3.04% for the standard PSO algorithm and 5.45% for the ABC algorithm. For mass-controlled OTA, the mean design error for MPSO is 1.32%, compared to 4.70% for the ABC algorithm and 5.63% for the standard PSO algorithm.

G. Wu et al. (2016)In this study, we propose a population-based approach to implement a set of multiple strategies, creating a new DE variant called Multi-Population-Set DE (MPEDE) which consists of three mutation strategies simultaneously, e.g. ie "Current-to -pbest / 1" and "current-to-rand / 1" and "rand / 1". There are three smaller indicator subpopulations of equal size and a much larger reward subpopulation. Consequently, better mutation strategies adaptively acquire more computational resources during evolution. The control parameters of each mutation strategy are also adjusted independently.

Mansour Barari et al. (2014)this article examines a scalable design system for automated sizing of analog integrated circuits (ICs). The results show that the design specifications are met exactly. Comparisons with available methods such as genetic algorithms show that the proposed algorithm offers significant advantages in terms of the quality and robustness of the optimization. Furthermore, the algorithm is proven to be efficient.

PURPOSED CMOS VOLTAGE REFERENCE CIRCUIT

The circuit configuration of the CMOS voltage reference shown in Fig. 3 can be divided into three parts. The first part consists of the transistors M1, M3 and R1 to generate the current with a negative temperature coefficient (I_{CTAT}), the second part consists of the transistors M2 and R2 to generate the current with a positive temperature coefficient (I_{PTAT}) and the last part is a current mirror circuit consisting of the transistors M4, M5 and M6. M4 is set to sum the current of ICTAT and IPTAT, which is independent of temperature and reflected on M6 to generate the voltage reference (V_{ref}).

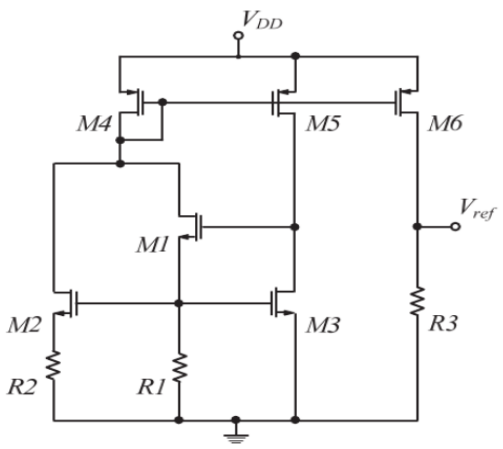

Fig. 3 Proposed Voltage Reference Circuit

In the first part, the M1 and M3 are defined to operate in saturation and weak inversion region, respectively. Then, the drain current of M1 and the gate-source voltage of M3 (M_{3gsV}) is given by

$$I_{D_{M1}} = \frac{1}{2} m_p C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$V_{gs_{M3}} = nV_T \ln\left[\frac{I_{ds3}.L_3}{I_t.W_3}\right] + V_{th}$$

Where V_T is the thermal voltage, can be written as

$$V_T = \frac{kT}{q}$$

Where k is the Boltzmann's constant (1.38 x10-23 J/K), q is electric charge (1.6 x10-19 C) and T is absolute temperature. The drain current of M3 is expressed in term of exponential can be expressed as

$$I_{ds3} = I_t \frac{W_3}{L_3} e^{\frac{q(V_{gs_{M3}} - V_{th})}{nkT}}$$

Where Vth is the threshold voltage, $W_3$and L_3 is channel width and channel length of MOS transistor, respectively.

$$I_t = 2nm_n C_{ox} \left(\frac{kT}{q}\right)^2$$

Where It is the saturation current of the MOS transistor, n is the slope factor, Coxis the gate oxide capacitance per unit area and μ is the electron mobility

$$\frac{\partial V_{gs_{M3}}}{\partial T} = \frac{V_{gs_{M3}}}{T} - 2n\frac{k}{q}$$

When increasing temperature the Vgsof MOS transistor M3 will be decreased which is called V_{CTAT} and the I_{CTAT} is expressed by.

$$I_{CTAT} = \frac{V_{gs_{M3}}}{R1}$$

In the second part, from the circuit as shown in fig. 2 the M2 is defined to operate in weak inversion region and V_{R1} is equaled to $V_{GS2} + V_{R2}$. So the voltage drop across R_2 can be written as

$$V_{R2} = nV_T \ln m$$

Where m is aspect ratio of MOS transistors M2 and M3, and $I_{R2}$is proportional to V_T, can be written as

$$I_{PTAT} = I_{R2} = \frac{nkT}{R2q} \ln m$$

found that the current I_{R2} has a positive temperature coefficient; it's clearly seen that when increasing temperature, the current I_{R2}will be increased. In the last part, the current mirror circuit is composed of transistors M4, M5 and M6. The MOS transistor M4 is defined for summing the current of $I_{CTAT}$and I_{PTAT} which is independent of temperature, can be expressed as

$$I_{ref} = I_{CTAT} + I_{PTAT}$$

$$I_{ref} = \frac{V_{gs_{M3}}}{R1} + \frac{nV_T}{R2} \ln m$$

The current$I_{ref}$is mirrored from M4 to M6, then the reference voltage can be obtained as follow.

$$V_{ref} = I_{ref} R3$$

PRINCIPLE OF VOLTAGE REFERENCE CIRCUIT

The principle of operation of a voltage reference suggests two parts of the circuit as shown in Fig. The first circuit generates the voltage with a negative temperature coefficient of about -2 mV/ °C, it is called complementary to absolute temperature (C_{TATV}) and the other circuit generates the voltage with a positive temperature coefficient of about 0.086 mV / ° C multiplied by the gain K, which is proportional to the absolute temperature (P_{TATV}).

The reference voltage generator is added by the C_{TAT} and P_{TAT} currents to generate a reference current (I_{ref}) which is used to generate the reference voltage (V_{ref})

$$V_{ref} = (I_{CTAT} + KI_{PTAT})R_{ref}$$

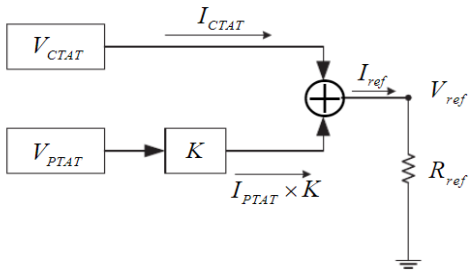

Fig. 4: Block diagram of a voltage reference circuit

For temperature compensation of the reference voltage, a zero temperature coefficient must be achieved under the following conditions

$$\frac{\partial V_{ref}}{\partial T} = 0$$

The voltage reference with a temperature coefficient (TC) is defined by the min / max limits of the rated output voltage in the operating temperature range as follows.

$$TC = \frac{1}{V_{atroomtemp}} \left[\frac{V_{\max} - V_{\min}}{T_{\max} - T_{\min}} \right] .10^6 \; ppm / °C$$

The voltage reference circuit exhibits a TC limit typically between 20 to 100 ppm/°C.

HIGH POWER SUPPLY REJECTION RATIO

The PSRR in the proposed structure is improved by using the regulated voltage of V_{reg}. The mirror currents in the transistors M6 and M7 provide the regulated voltage V_{reg} as power to the core. The current source Ib is independent of the supply voltage and a fraction of the current flowing through M1-M4. This structure separates the regulated voltage and the supply voltage. This structure separates the regulated voltage from the supply voltage. Compared to conventional bandgap circuits, in this structure, the necessary decrease of the supply voltage is equal to the drain-source voltages of M6 and M7. Also, M8 is preloaded in cascade configuration along with M1-M4. The effects of the noise of the supply voltage on the regulated voltage V_{reg} are mitigated by the following techniques.

1. Using Cascade current source configuration.

2. Utilizing a feedback loop. Feedback loop in Vreg node using a high gain op-amp amplifies the voltage difference between +in and –in nodes.

VOLTAGE REFERENCE ARCHITECTURES

Voltage references are one of the most commonly used blocks in several PVT insensitive current references. There are several desirable properties for a very high quality voltage reference. The reference needs to provide a truly constant voltage under many different conditions. Changes in the supply voltage must not lead to significant changes in the reference output voltage. The results of the temperature at the exit of the device should also be minimal. Finally, 2 identical references with similar technology must have similar output properties. There are many completely different strategies for planning a tension baseline. Among these, there are 3 main

classes that will compose the different styles. These categories generally describe either the technology in which the reference is built or the method for deriving the constant output voltage. In MOS technologies, the most obvious way to derive a reference is to use the on-board voltage. Very correct references usually use buried Zener diodes. In strictly bipolar processes, the emitter-base junction of a BJT does not derive the silicon band gap voltage, which must be used as the reference voltage. Finally, in a very MOS process, it is possible to form equal bipolar transistors to extract the band gap voltage from the silicon. These are used with various MOS circuits to provide a reference voltage.

CURRENT REFERENCE ARCHITECTURE

A current architecture for generating a power source is shown below. This architecture is only concerned with the conversion between a voltage level and its power supply. This topology requires a bandgap reference and results in a specific energy dump in node 1.

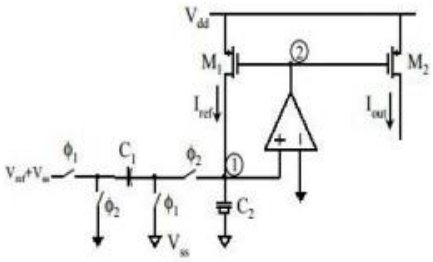

Fig. 1. Current Reference Architecture

During ϕ1, C1 charges to Vref. During ϕ2 this charge is dumped on node 1. Thus, the ripple voltage is –

$$\Delta V = -\left(\frac{2C1}{C1 + 2C2}\right) Vref$$

The ripple voltage can be reduced by increasing the value of C2. A large C2 is reduced in the case of ripple to the detriment of an enlarged matrix area. The current delivered by the switched capacitor is approximately.

$$Iref = C1 * Vref * Fclk$$

This architecture offers 0.029% accuracy. A further improvement of this topology can be achieved by placing an amplifier connected to M2 to increase the output resistance. Another improvement is the addition of a filter between the output of the amplifier, node 2, and the gate of M2.

CONCLUSION

Circuit design, especially for the difficult design of an analog integrated circuit (IC) as a voltage reference circuit with complex structures and parameter expansions, must consider many factors

such as power consumption. Power, bandwidth, stability and production range at the same time. The circuit designer finds optimum performance through precise calculations and parameterizations, which take time and effort, and the automatic design would help the designer easily find the optimum point. Therefore, automatic design is required for analog integrated circuits. Using the proposed algorithm is said to improve line sensitivity, temperature coefficient, performance and chip area. This article briefly examines the voltage reference architecture and the current reference architecture. The intended CMOS voltage reference circuit and the voltage reference circuit principle are described in this paper.

REFERENCES

1. Xiangping Li, Guangming Dai "An Enhanced Multi-Population Ensemble Differential Evolution", CSAE 2019: Proceedings of the 3rd International Conference on Computer Science and Application EngineeringOctober 2019 Article No.: 14 Pages 1–5.
2. Y. Zeng, X. Zhang, and H.-Z. Tan, ''A 86 nA and sub-1 V CMOS voltage reference without resistors and special devices,'' in Proc. IFIP/IEEE Int. Conf. Very Large Scale Integr. (VLSI-SoC), Oct. 2017, pp. 1–5.
3. Subhash Patel, Rajesh A Thakker "Automatic Circuit Design and Optimization using Modified PSO Algorithm", Journal of Engineering Science and Technology Review 9 (4) (2016) 192- 19.
4. G. Wu, R. Mallipeddi, P. N. Suganthan, R. Wang, and H. Chen, ''Differential evolution with multi-population based ensemble of mutation strategies,'' Inf. Sci., vol. 329, pp. 329–345, Feb. 2016.
5. Mansour Barari, Hamid Reza Karimi "Analog Circuit Design Optimization Based on Evolutionary Algorithms", Mathematical Problems in Engineering, 2014.
6. P. Civicioglu, E. Besdok, "A conceptual comparison of the cuckoosearch, particle swarm optimization, differential evolution and artificial bee colony algorithms", Artificial Intelligence Review 39 (4) (2013) 315-346
7. P. Pereira, M. Kotti, H. Fino, M. Fakhfakh, "Metaheuristic algorithms comparison for the lc-voltage controlled oscillators optimal design", in: Modeling, Simulation and Applied Optimization (ICMSAO), 2013 5th International Conference on, IEEE, 2013, pp. 1-6.
8. M. Barros, J. Guilherme, N. Horta, "Analog circuits optimization based on evolutionary computation techniques", INTEGRATION, the VLSI journal 43 (1) (2010) 136-155.
9. R. A. Thakker, M. S. Baghini, M. B. Patil, "Automatic design of low-power low-voltage analog circuits using particle swarm optimization with re-initialization", Journal of Low Power Electronics 5 (3) (2009) 291-302.
10. Y. Del Valle, G. K. Venayagamoorthy, S. Mohagheghi, J.-C. Hernandez, R. G. Harley, "Particle swarm optimization: basic concepts, variants and applications in power systems", Evolutionary Computation, IEEE Transactions on 12 (2) (2008) 171-195.
11. G. Nicosia, S. Rinaudo, E. Sciacca, "An evolutionary algorithmbased approach to robust analog circuit design using constrained multi-objective optimization", Knowledge-Based Systems 21 (3) (2008) 175-183.
12. A. Somani, P. P. Chakrabarti, A. Patra, "An evolutionary algorithmbased approach to automated design ofanalog and rf circuits using adaptive normalized cost functions", Evolutionary Computation, IEEE Transactions on 11 (3) (2007) 336-353.