

## Analysis of Narrow Channel Single Gate Fully Depleted SOI MOSFET

**Prashant Mani**

Assistant Professor

Department of Electronics and Communication Engineering

SRM University NCR Campus

Modinagar

**Shivam Sharma**

M.Tech Scholar

### ABSTRACT:

In the present paper we analyze the electrical characteristics of single gate fully Depleted SOI MOSFET. This paper were focused on following electrical characteristics that are threshold voltage, Short Channel Effect, Substrate Current, Heating Effect, Doping Effect, Kink Effect of single gate FDSOI MOSFET. The device structure and characteristics were constructed examined and simulated using Silvaco Atlas.

**Keywords**— SOI Technology, Fully Depleted SOI MOSFET, Silva co Software

### I. INTRODUCTION

Over the past decades transistors have been scaled down in size to increase performance and reduce power consumption, leading to better electronics devices for digital application. Historically it has been seen from the last many years that scaling, i.e. reduction of physical dimensions of the transistor structure has always improved the performance of devices, and also its density scaling also leads to increases of the circuit speed and decrease of the power consumption and area occupied by circuit.

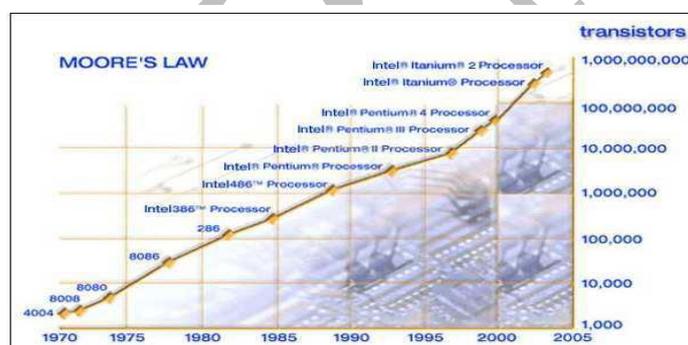


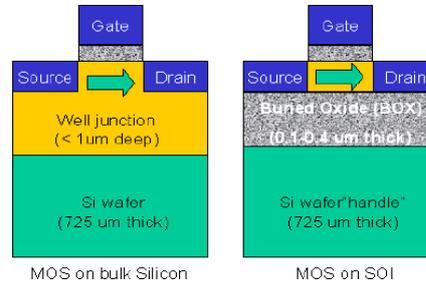
Figure 1:- Moore's Law

Scaling of MOSFET device is required to increase the device speed and packaging density, but it degrades the device performance. In order to continue to deliver higher performance, while keeping the leakage under control bulk silicon transistors have become even more complex adding additional manufacturing steps. The bulk devices in the microelectronics industry having same undesirable effects like latch up and parasitic capacitance between source and drain and substrate, both of result from lack of electrical isolation between the active device and the substrate.

SOI enables increased chip functionality without the cost of major process equipment changes (such as higher resolution and lithography tools). The advantages of IC devices built on SOI wafers (mainly higher circuit performance and lower operating voltages) have produced a powerful surge in the performance of high speed network and new design for hand held computing and communication devices with longer battery life.

## II. THE SOI MOSFET

The SOI devices are little bit different from bulk CMOS. Silicon on Insulator (SOI) wafers consist of three layers: a thin (200Å to several microns, depending on the application) layer of single crystal silicon on a thick (1000Å to 4000Å) silicon dioxide layer that is bonded to a conventional to “handle” wafer. The entire transistor are is located in thin top layer of silicon and electrically isolated from bulk wafer by the buried oxide (BOX) layer. fig 2



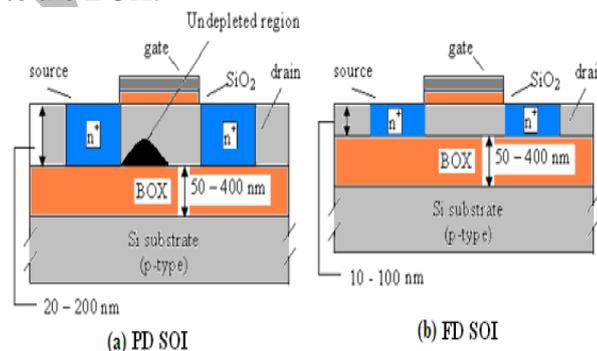
**Figure 2:- Sketch of Metal Oxide Semiconductor transistor on a bulk silicon wafer (left) a on – insulator (SOI) wafer (right)**

In an MOS transistor formed by on an SOI wafer, the entire transistor is in (usually less than 0.2 μm thick) silicon layer insulator from the bulk of the silicon “handle” wafer by a thick (usually 0.1 to 0.4 μm) oxide. The smaller volume of of silicon that is depleted during Switching of an SOI transistor increase the speed of signal processing an allow operation at lower drive voltages.

As shown in fig:-1 the transition from micro technology to nanotechnology has already happened in 2002, also as predicted by Moore the scaling down process increase the circuit speed while reducing the cost drastically, preserving the transistor performance with scaling down was the key of microelectronics technology evolution and its success.

As the continuous down are two types of SOI devices PDSOI (Partially Depleted SOI) and FDSOI (Fully Depleted SOI). For a n-type PDSOI MOSFET the sandwiched P-type film between the gate oxide (GOX) and buried oxide (BOX) is large, so that the depletion region can not cover the whole P region so some extent PDSOI behaves like bulk MOSFET.

Obviously there some advantages over bulk MOSFETs, the film is very thin in FDSOI devices so that the depletion region covers the whole film. In FDSOI MOSFET the front gate (GOX) supports the less depletion region covers the whole film. In FDSOI the front gate (GOX) supports less depletion charges than the bulk so an increase in inversion charges occurs is in higher switching speed. Other drawbacks in bulk MOSFETs, like threshold voltage roll off, higher sub threshold slop body affected are reduced in FDSOI since source and drain electric field cannot interfere due to the BOX.



**Figure 3:- A cross view for a (a) Partially depleted and (b) a fully depleted SOI MOSFET**

The main problem in PDSOI is the Floating Body Effect (FBE) since film is not connected to the any of the supplies. FDSOI MOSFETS has the advantage of lower parasitic capacitance and better sub threshold swing, reducing short channel effect (SCE) and free from kink effect.

### III. DEVICE STRUCTURE AND SIMULATION

Simulation of single gate fully depleted SOI n-MOSFET (silicon film thickness=0.02 $\mu\text{m}$ ) were performed by the silvaco atlas tools. Typical values of various transistor parameters used in this simulation are shown in these simulation are shown in Table 1.

**Table 1: Parameters of Single Gate SOI n MOSFET Transistor**

Symbol	Description	Value
$L_D, L_S, L_G$	Drain length, Source length, Gate length	0.11[ $\mu\text{m}$ ],0.11[ $\mu\text{m}$ ],0.10[ $\mu\text{m}$ ]
L	Channel length	0.10[ $\mu\text{m}$ ]
$T_{OX}$	Gate Oxide Thickness	0.01[ $\mu\text{m}$ ]
$T_{SI}$	Silicon film Thickness	0.02[ $\mu\text{m}$ ]
$T_{BOX}$	Buried oxide Thickness	0.04[ $\mu\text{m}$ ]
	Substrate Thickness	0.120[ $\mu\text{m}$ ]
$N_A$	Substrate Concentration	$1 \times 10^{18} [\text{cm}^{-3}]$
$N_D$	Drain & source concentration	$1 \times 10^{20} [\text{cm}^{-3}]$

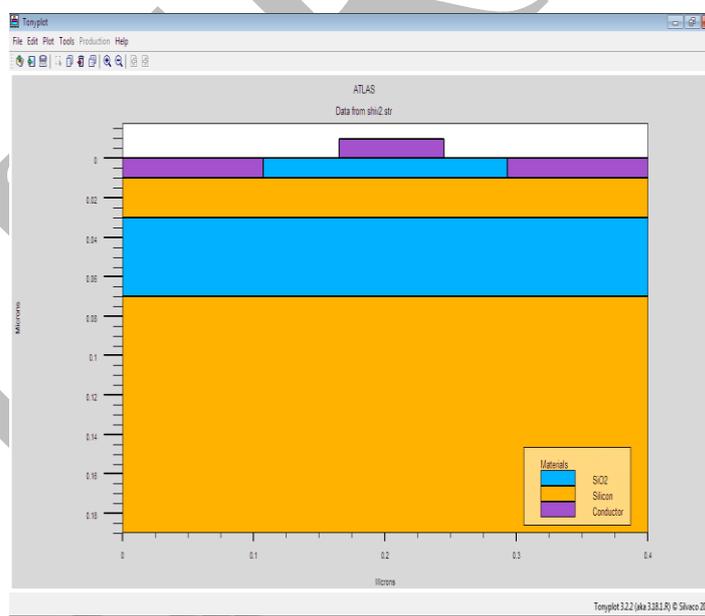


Figure 4:- Device Structure of the Single Gate FDSOI n-MOSFET with effective channel length 0.1 $\mu\text{m}$  channel doping is  $1 \times 10^{18} \text{cm}^{-3}$  and drain and source doping concentration is  $1 \times 10^{20} \text{cm}^{-3}$  gate oxide thickness is 0.01 $\mu\text{m}$

### IV. RESULT AND DISCUSSION

From Fig 5 presents  $I_d$ - $V_{gs}$  characteristics of narrow channel single gate FDSOI n-MOSFET. We see that threshold voltage at  $V_{ds}=1.5\text{v}$  is more than at  $V_{ds}=0.1\text{v}$ . It shows that as we increase the  $V_{ds}$  the threshold voltage of FDSOI n-MOSFET is increase.

From Fig 6 presents Id-Vds characteristics of narrow channel single gate FDSOI n-MOSFET. It shows that Id-Vgs characteristics at Vds=1.5v is much better at Vds=0.1v. It shows that as we increase the Vds the Id-Vds characteristics of FDSOI n-MOSFET is much sharper than previous one and we see that there is no kink in Single gate FDSOI n-MOSFET.

From Fig 7 presents Id-Substrate current characteristics of narrow channel single gate FDSOI n-MOSFET. It shows that as we increase Vgs, we see that Id-substrate characteristics (at Vgs=1.7) is much more enhanced and less ambiguous than previous one (at Vgs=0.8).

From Fig 8 shows the Net Doping Effect of narrow channel single gate FDSOI n-MOSFET channel length of 100nm. Here we use the channel doping is  $1E18cm^{-3}$  and drain and source doping concentration is  $1E20cm^{-3}$ .

From Fig 9 shows the Lattice Heating Effect of narrow channel single gate FDSOI n-MOSFET channel length of 100nm, which is much more effect than conventional MOSFET. From our analysis we observed that FDSOI MOSFET gives improved better results than PDSOI MOSFET.

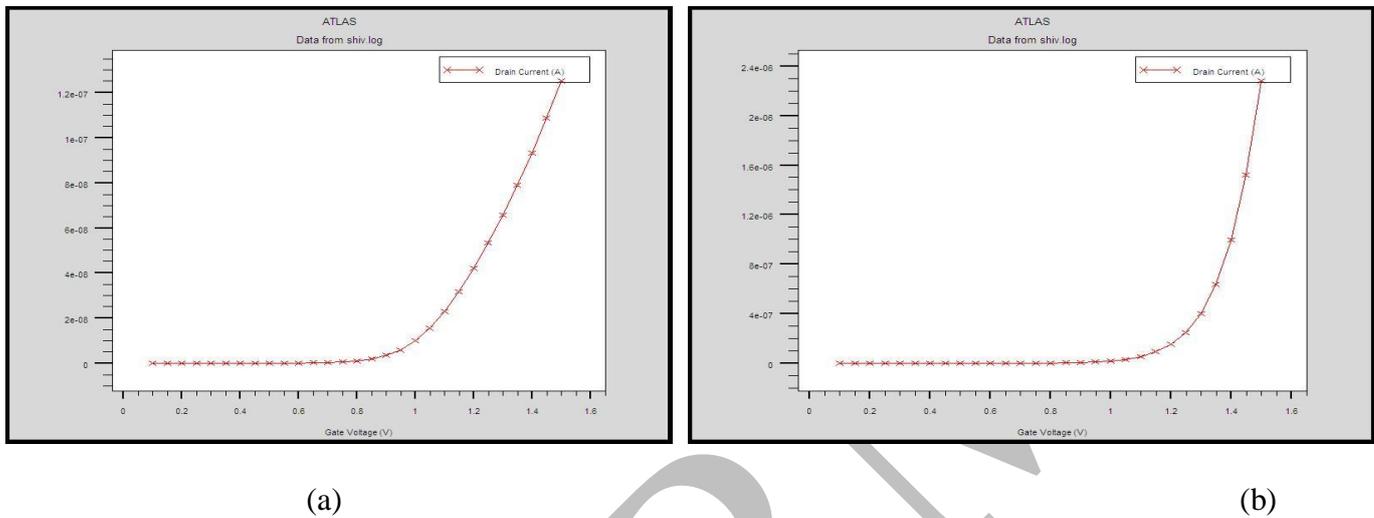


Figure 5:- Id-Vgs Characteristics of Single Gate FDSOI n-MOSFET at (a) Vds=0,1v (b) Vds=1.5v respectively.

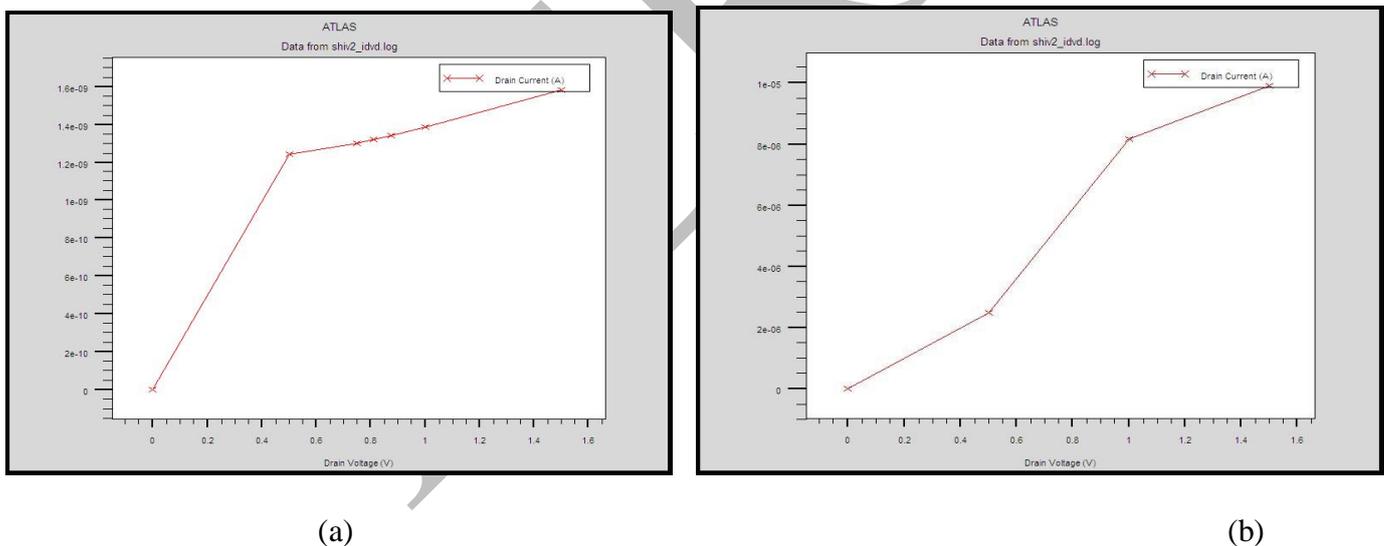
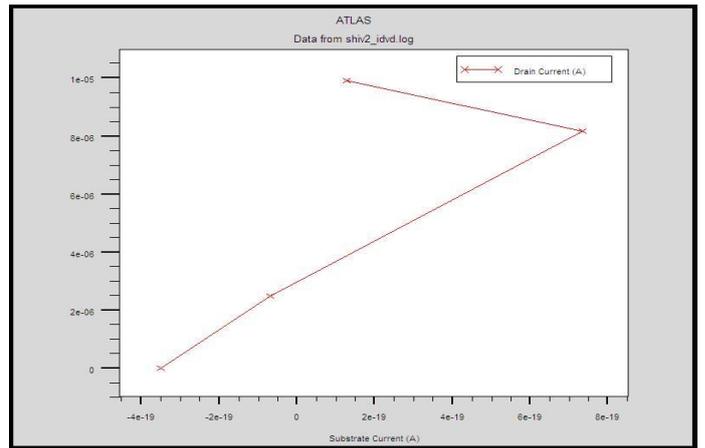
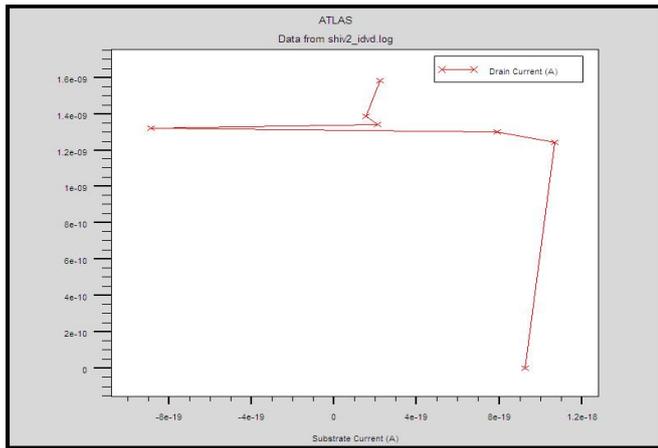


Figure 6:- Id-Vds Characteristics of Single Gate FDSOI n-MOSFET at (a) Vgs=0,8v (b) Vgs=1.7v respectively and analysis of Kink effect in FDSOI MOSFET & there is no kink effect in FDSOI n-MOSFET.



(a)

(b)

Figure 7:- Id-Substrate Current Characteristics of Single Gate FDSOI n-MOSFET at (a)  $V_{gs}=0.8v$  (b)  $V_{gs}=1.7v$  respectively.

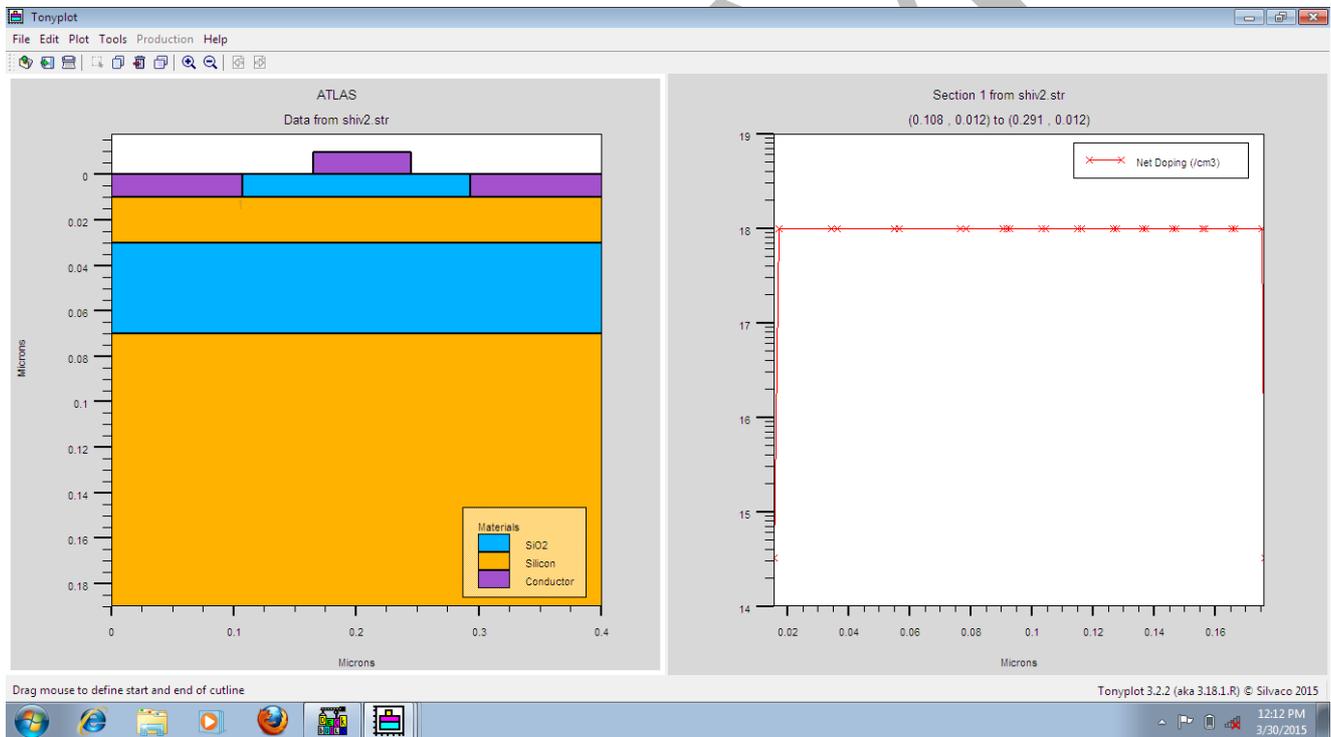
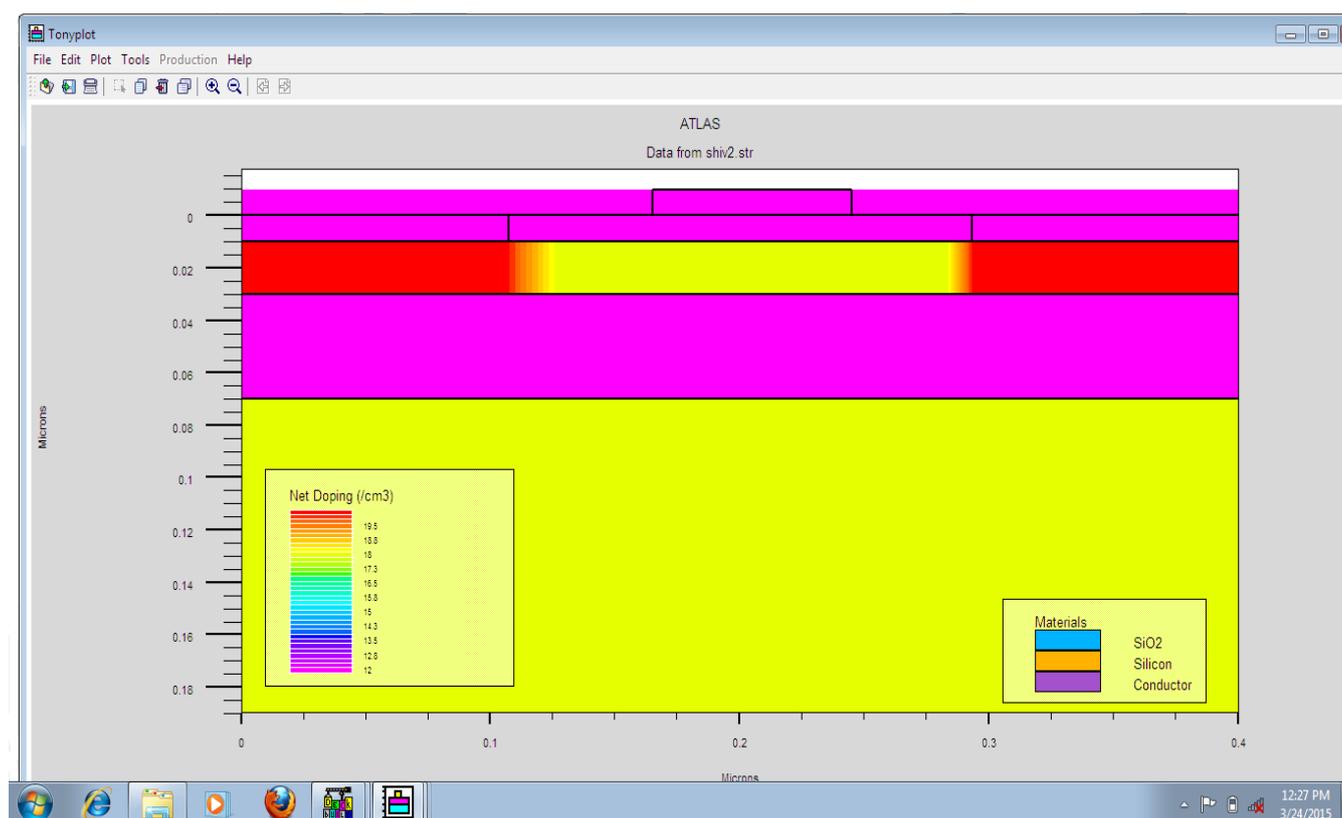


Figure 8:- Net Doping Effect of Single Gate Fully Depleted SOI n-MOSFET Channel Length of 100nm



**Figure 9:- Lattice Heating Effect of Narrow Channel of Single Gate Fully Depleted SOI n-MOSFET Channel Length of 100nm**

## VI. CONCLUSION

In this paper we successfully obtained the electrical characteristics of narrow channel single gate fully depleted MOSFET. The characteristics of FDSOI MOSFET are obtained using silvaco atlas software. Here we see that the electrical characteristics of FDSOI MOSFET is much better than PDSOI MOSFET. As the device shrinks, the short channel effects (SCE) of FDSOI MOSFET are very important in conventional MOSFET, the short channel effects (SCE) of FDSOI MOSFET is much better than conventional and PDSOI MOSFET. In the above analysis we obtained improved electrical characteristics of FDSOI MOSFET (like:- Lattice heating effect, Net doping effect, Kink effect) as compared to PDSOI MOSFET. The major drawback of PDSOI n-MOSFET is kink effect, which is eliminated in FDSOI n-MOSFET.

## REFERENCES

1. The International technology Roadmap for semiconductor, Emerging Research Devices, 2009.
2. C.T Sah, A History of MOS Transistor Compact Modeling, Proc.Tech.WCM 2005, 347-385, 2005.
3. B.R Nag, Physics of quantum well devices, (Kluwer Academic, THE Netherlands), 2000.
4. J.P Colinge, Tyndall National Institute, "The New Generation of SOI MOSET", Romanian journal of information, science and technology, 11, number 1, 2008, 3-15.
5. Rohit S. Shenoy, Technology and scaling of ultra thin body Double-Gate FETs.
6. Silvaco, ATLAS User's Manual.
7. Semiconductor Devices, S.M.sze.
8. FZ.Rahou, A.Guan-Bouazza, M.Rahou, "Electrical characteristics Comparison between Fully- Depleted and SOI MOSFET and Partially-SOI MOSFET using Silvaco Software" GLOBAL JOURNAL OF RESEARCHES IN ENGINEERING ELECTRICAL AND ELECTRONICS ENGINEERING( 0975-5861) Volume 13 Issue 1 Version 1.0 Year 2013. Online ISSN:2249-4596.